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| Serial No: |
| **Midterm Exam** |
| **Total Time: 2 Hours** |
| **Total Marks: 65** |
| \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_  Signature of Invigilator |

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| **EE-227: Digital Logic Design** |
| Wednesday, 20th March, 2019 |
| **Course Instructors** |
| Mehreen Alam, Dr. Mehwish Hassan, Sana Hassan, Adnan Saeed |

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| **\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**  Student Name Roll No Section Signature |

## DO NOT OPEN THE QUESTION BOOK OR START UNTIL INSTRUCTED.

**Instructions:**

1. Attempt on question paper. Attempt all of them. Read the question carefully, understand the question, and then attempt it.
2. No additional sheet will be provided for rough work. Use the back of the last page for rough work.
3. If you need more space write on the back side of the paper and clearly mark question and part number etc.
4. After asked to commence the exam, please verify that you have **fourteen** (14) different printed pages including this title page. There are a total of **seven** (7) questions.
5. **Calculators are not allowed**.
6. Use permanent ink pens only. Any part done using soft pencil will not be marked and cannot be claimed for rechecking.
7. Understanding the question is the part of examination. Invigilator is not supposed to answer any questions.

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|  | **Q-1** | **Q-2** | **Q-3** | **Q-4** | **Q-5** | **Q-6** | **Q-7** | **Total** |
| **Marks Obtained** |  |  |  |  |  |  |  |  |
| **Total**  **Marks** | **10** | **06** | **08** | **10** | **10** | **15** | **06** | **65** |

**Question 1 Max Marks [10]**

1. The state of an 8-bit register is 1001 0111. What are its content if it represents: [2]
   1. Two decimal digits in BCD \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
   2. A binary number \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
2. Subtract the following numbers using 7-bit 2’s complement. [2]
   1. 54 - 32
   2. 0 - 4
3. (627.356)8 = ( \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ )16 [2]
4. (10011000) BCD + (01011000) BCD = (\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ ) BCD [2]
5. Convert **(-248)10** to [2]
   1. 10-bit binary signed magnitude
   2. 1’s complement 10-bit binary representation.

**Questions-2 Max Marks [6]**

1. Using postulates and theorems of Boolean algebra and reduce the expression for F to minimum number of literals. [2]

F = x’y’z’ + x’y’z + x’yz’ + x’yz + xy’z

1. Convert (show the working) the given expression (b+c’)(a)(a+b’)+a’ to: [4]
   1. standard SOP \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
   2. standard POS \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
   3. canonical SOP \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
   4. canonical POS \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**Question-3 Max Marks [8]**

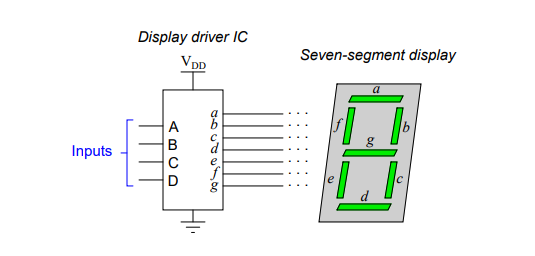
Answer the questions for the truth table below.

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | C | D |  |  | | Y | | Z |
| 0 | 0 | 0 | 0 |  |  |  | | 1 | 0 |
| 0 | 0 | 0 | 1 |  |  |  | | 0 | 0 |
| 0 | 0 | 1 | 1 |  |  |  | | 1 | 0 |
| 0 | 0 | 1 | 0 |  |  |  | | 0 | 0 |
| 0 | 1 | 1 | 0 |  |  |  | | 1 | X |
| 0 | 1 | 1 | 1 |  |  |  | | 1 | X |
| 0 | 1 | 0 | 1 |  |  |  | | 1 | X |
| 0 | 1 | 0 | 0 |  |  |  | | 1 | X |
| 1 | 1 | 0 | 0 |  |  |  | | 1 | 0 |
| 1 | 1 | 0 | 1 |  |  |  | | 0 | 0 |
| 1 | 1 | 1 | 1 |  |  |  | | 1 | 0 |
| 1 | 1 | 1 | 0 |  |  |  | | 0 | 0 |
| 1 | 0 | 1 | 0 |  |  |  | | 0 | 1 |
| 1 | 0 | 1 | 1 |  |  |  | | 1 | 0 |
| 1 | 0 | 0 | 1 |  |  |  | | 0 | 1 |
| 1 | 0 | 0 | 0 |  |  |  | | 1 | 1 |

1. Write the Prime Implicants for Y [2]
2. Write the essential Prime Implicants for Y [2]
3. Write the output Z in the form of max-terms [1]
4. Draw the **simplified** combinational circuit for “Y” using NAND gates only. [3]

**Question-4 Max Marks[4+6]**

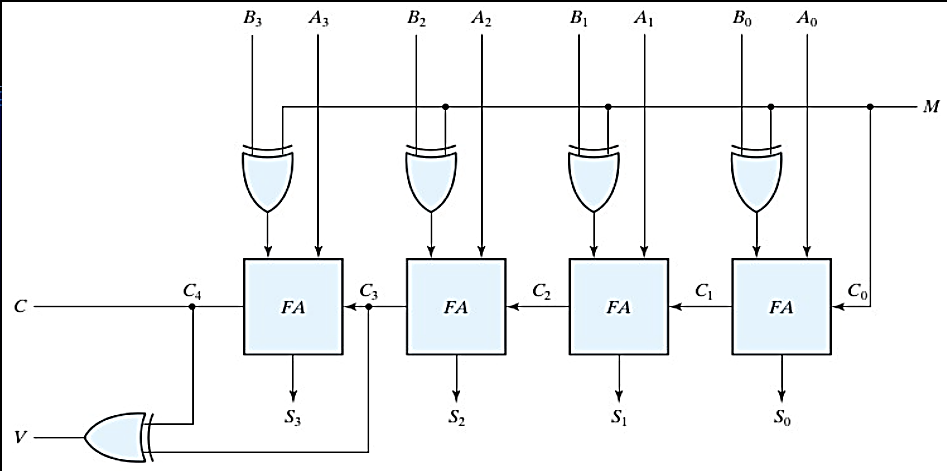
A seven segment decoder is a digital circuit designed to drive a very common type of digital display device (shown below) a set of LED (or LCD) segments that render numerals 0 through 9 at the command of a four-bit BCD code. **Complete the truth table** for this and **draw the logic diagram** for simplified expression of ‘a’ , ‘f’ only. The first row of the table is already filled in.



|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | C | D | a | b | c | d | e | f | g | Display |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | “ 0” |
|  |  |  |  |  |  |  |  |  |  |  |  |
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**Question-5 Max Marks [10]**

For the following 4 bit Adder circuit (where A= A3A2A1A0 & B= B3B2B1B0), modify the circuit (on top of the logic diagram given below) so that is performs both **addition** and **subtraction**. Use M as a control bit, where M=0 performs addition and M=1 performs subtraction. Also perform the following operations and show the values of S0, S1, S2 ,S3 , C and V for each case . [4+6]



a) Unsigned numbers (M=0 , A=+7 ,B=-2)

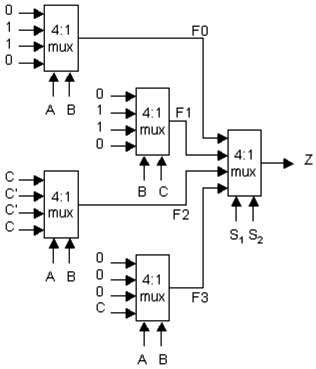
b) Signed numbers (M=0, A=+7, B=-2)

c) Unsigned numbers (M=1, A=+7 ,B=-2)

d) Signed numbers (M=1, A=+7, B=-2)

**Question-6 Max Marks [15]**

**(a)**  The following circuit implements a Boolean function of 5 variables (A, B, C, S1, and S2).  It uses five 4:1 multiplexers.  Note that S1 and S2 are simply used to select one of four functions of A, B, and C.  Write the equations for these four functions.  We’ll call them F0, F1, F2, and F3.  Inputs to the multiplexer are numbered from 0 to 3 top to bottom, control inputs are high-order on the left (Most significant bit), low-order (least significant bit) on the right.  [8]



F0= \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

F1=\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

F2=\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

F3=\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(b)**

Implement the given Boolean function Using one **4x1 Multiplexer** and **external gates**

**F(A, B,C,D) = BD + B′D′ + CD + AD** [7]

**Question-7 Max Marks [6]**

Fill in the following priority table for an eight-bit priority encoder with the following priorities:

**D1 > D2 > D6> D3 > D0> D4 > D5 > D7**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Inputs | | | | | | | | Outputs | | |
| D0 | **D1** | **D2** | **D3** | **D4** | **D5** | **D6** | **D7** | **x** | **y** | **z** |
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ROUGH WORK

BEST OF LUCK